

ABSTRACT OF THE DISCLOSURE

This invention provides a micro controller in which a JTAG (Joint Test Action Group) port becomes available through a specific operation even after a security bit is set. More specifically, an embodiment of this invention provides a micro controller wherein: when an address signal AD2 and data DT2 are input from a JTAG port 11, the address signal AD2 and data DT2 are kept in shift registers 25 and 26 through a TAP (Test Access Port) 24; the address signal AD2 is forwarded to a flash ROM and data DT1 of the address specified by the address signal AD2 is read out and output a comparator 27; the data DT2 is also output the comparator 27; ~~when~~ if the data DT1 and DT2 agree, the output signal from the comparator 27 turns "H" and the output signal from ~~the~~ an AND gate 23 turns "L" independent of a security signal SEQ; and ~~hereby the~~ thereby a JTAG control circuit 12 ~~turns switch-on~~ is switched on and the JTAG port 11 becomes connected to ~~the TAP~~ TAPs 13 and 14 through the JTAG control circuit 12.

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This invention provides a micro controller in which a JTAG (Joint Test Action Group) port becomes available through a specific operation even after a security bit is set. More specifically, an embodiment of this invention provides a micro controller wherein: when an address signal AD2 and data DT2 are input from a JTAG port 11, the address signal AD2 and data DT2 are kept in shift registers 25 and 26 through a TAP (Test Access Port) 24; the address signal AD2 is forwarded to a flash ROM and data DT1 of the address specified by the address signal AD2 is read out and output a comparator 27; the data DT2 is also output the comparator 27; if the data DT1 and DT2 agree, the output signal from the comparator 27 turns "H" and the output signal from an AND gate 23 turns "L" independent of a security signal SEQ; and thereby a JTAG control circuit 12 is switched on and the JTAG port 11 becomes connected to TAPs 13 and 14 through the JTAG control circuit 12.